Amendments to the Specification:

Please replace paragraph **[0013]** on page 6 with the following amended paragraph:

[0013] The circuit of the present invention has followed a multi-threaded approach to isolate the functional blocks to guarantee the retention of the embedded RAM data after and during the power up/down. 1) All circuitry related to the embedded RAM and isolation cell circuitry is placed in a separate chip area and has its own un-interruptible power supply (VDD_RAM) and separate ground (VSS_RAM) terminals, with separate N-well, substrate ties and guard rings. 2) Tri-state buffering is used to connect/disconnect the embedded RAM circuitry from the core logic and I/O interface circuits. 3) External signals are used to enable the tri-state buffer. Alternatively, internally generated signals may be used to enable the tri-state buffer (e.g., through internal testing circuitry). 4) Serially connected N-channel devices electrically connect the tri-state buffer ground. The serially connected N-channel devices are driven by the remaining power supplies (ALL OTHER POWER SUPPLIES) on the chip (i.e., VDD_I/O, VDD_Core, VDD_Analog, etc.). Only if all remaining power supplies are turned on will the tri-state buffer be enabled after connecting to its ground (VSS_RAM). None of the transients on the individual power supplies can enable the tri-state buffer because the EN_EXT1 keeps the ground disconnected from the tri-state buffer. Any power supply transients that occur during the re-connection to the main PCB are shielded from affecting the tri-state buffer by serial N-channel device MN3 by the low state of EN_EXT1 signal. 5) After latching the last logic state into the transparent latch, the tri-state buffer is tri-stated and the latch or keeper cell maintains the last state. 6) Even if the printed circuit board (PCB) were removed from the system while keeping the VDD_RAM power supply turned on, the external enable signals EN_EXT1 and EN_EXT2 maintain their low state by means of pull-down resistors RP1 and RP2. Thus, the Isolation Cell remains active, isolating the embedded RAM circuitry from all other power supply and all interfacing signal transients. 7) The RAM outputs are connected to the core and/or to the I/O interface circuits by Isolation Cells, as shown in FIGs. 2-5. 8) Excessive voltage overshoot/undershoot on the normal power supplies during the power-

up and power-down transients are clamped by input protection diodes or transistors. As long as both external enable signals EN_EXT1 and EN_EXT2 maintain logic low states, the N-channel device MN3 remains OFF and disconnects any transient currents/voltages from MN1, MN2, and MNx NMOS transistors or other N-channel devices.

Please replace paragraph **[0014]** on page 7 with the following amended paragraph:

[0014] The present invention is directed to integrated circuit applications having multiple power supplies. Most of the present integrated circuits have separate power supplies for Input/Output (I/O) receivers and drivers, and for so called core, the internal logic circuitry of the chip. At least two separate power rails are provided in such case. An example of such multiplicity is the 3.3 volt power supply for I/O circuitry (VDD_I/O) and a 1.8 volt power supply ~~volts~~ for powering the core circuitry (VDD_Core). Still other power supplies are provided for unique functions such as PLL (VDD_Analog), etc. The justifications for separate power supplies are dictated for 1) lowering the power dissipation of core, 2) separating of large currents of switching output drivers, 3) lowering the ground bounce and power rail overshoot, 4) minimizing the crosstalk and coupling into the analog circuitry, etc.

Please replace paragraph **[0017]** on page 9 with the following amended paragraph:

[0017] FIG. 2 shows a first embodiment of an isolation cell, Isolation Cell Type 1, of the present invention for an arbitrary input pin of the embedded RAM. It is understood that a set of eight, sixteen, twenty, or another number of isolation cells may be used for data transfer to and control signals for the embedded member. A different set of isolation cells may be used for the output from the embedded memory. In this embodiment, a totem pole arrangement of PMOS and NMOS transistors implement an enablement mechanism for writing to and reading from an embedded memory. A keeper cell consisting of two inverters is connected to the RAM input and to the tri-state buffer output. As long as the un-interruptible power supply VDD_RAM provides the power to the embedded circuitry, the last logic state will be maintained at that pin. In operation,

when enable signal EN_EXT2 is at a logic high, NMOS transistor MN4 and PMOS transistor MP1 are both turned on. The PMOS transistor MP1 is turned on because when enable signal EN_EXT2 is at a logic high level, inverter I1 provides a logic low level to the gate of PMOS transistor MP1. Similar to enable signal EN_EXT1, enable signal EN_EXT2 is tied to ground through pull down resistor RP1. Memory input signal RAM_IN is provided directly to the gates of PMOS transistor MP2 and NMOS transistor MN5. When RAM_IN is at a high logic level, a low logic level is latched by the keeper cell formed by inverters I2 and I3 that are electrically connected in parallel with the output signal line to the embedded RAM. The source of PMOS transistor MP1 is electrically connected to the embedded memory (i.e., RAM) dedicated power VDD_RAM.

Please replace paragraph **[0018]** on pages 10-11 with the following amended paragraph:

[0018] Other variations of the isolation cell may be employed. Various components, such as smoothing capacitors, transmission gates, and pull up resistors may be used in alternative embodiments, including variations of the isolation cell illustrated in FIGs. 2-5. A second embodiment of the isolation cell, Isolation Cell Type 2, of the present invention is shown in Figure 3. Instead of the keeper cell, a transparent latch L1 with inputs D, G and Q is used to store the last logic state of the particular RAM input. The latch control signal is connected ~~connect~~ to the G input to allow the last logic state of the tri-state buffer output to be stored in the transparent latch. The latch control signal can be generated in conjunction with external enable signals to ensure that last logic state is reliably stored. The transparent latch is powered by the VDD_RAM power supply. Alternatively, an edge triggered latch may be used. FIG. 4 shows a third embodiment in which the power level controlled transistors MN11, MN12, and MN13 serve as pass gates for an enable signal. The enable signal controls, the PMOS transistor MP12 and NMOS transistor MN14 to allow or prohibit passage of data signal RAM_IN. The output of transistors MN15 and MP11 is latched to stabilize the data for writing to the embedded memory. Optional capacitor C11 smoothes out the enable signal to eliminate glitches and prevent spurious data from being written to the embedded memory. Optional pull down

resistor RP11 ensures that the signal applied to switches MN14 and MP12 is never ambiguous in value. FIG. 5 illustrates an embodiment of the isolation cell in which each controlling tapped power level is fed to an inverter I21, I22, and I23 and controls one of multiple NMOS transistors MN21, MN22, and MN23 connected in parallel such that the drains are electrically connected to a common node and the sources are connected to a common ground VSS_RAM or a common negative power supply. The drains are electrically connected to pull up resistor RP21 which guarantees a high level input to AND gate U21 ~~is~~ if none of the transistors are turned on. The enable signal input, EN_EXT, coupled to a common ground VSS_RAM through RP22 and the embedded memory input RAM_IN are the other inputs to the AND gate U21. The output of the AND gate U21 is latched by pass through latch L22 or by bypass latch L21. Latches may be implemented as two inverters in tandem, two NAND gates in tandem, two NOR gates in tandem, a tandem combination of inverters, NAND gates and/or NOR gates, or the like. The latches may be D type flip flops. The latches may be transparent, level enabling, or clock edge triggered.

Please replace paragraph **[0021]** on pages 11-12 with the following amended paragraph:

[0021] FIG. 8 illustrates a flow chart of an embodiment of a method of the present invention. At the beginning 810, if any power supply that has been tapped by the isolation cell does not supply sufficient power 820, the isolation cell disables the embedded memory input and output 830. Otherwise, if there is data to transfer ~~830~~ 840, the isolation cell enables transfer of the data to the embedded memory ~~840~~ 850 and the transfer is performed ~~840~~ 860.